PAS106BCA-323 SINGLE-CHIP CMOS CIF COLOR DIGITAL IMAGE SENSOR
PAS106BBA-323 SINGLE-CHIP CMOS CIF B&W DIGITAL IMAGE SENSOR

General Description

The PAS106BCA-323/PAS106BBA-323 is a highly integrated CMOS active-pixel image sensor that has a CIF resolution of 356H x 292V. To have an excellent image quality, the PAS106BCA-323/PAS106BBA-323 outputs 10-bit RGB raw data through a parallel data bus. It is available in color or monochrome in 32-pin LCC package.

The PAS106BCA-323/PAS106BBA-323 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register sets, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **CIF(356 x 292 pixels) resolution, ~1/5" Lens**
- **Bayer-RGB color filter array**
- **On-chip 10-bit pipelined A/D converter**
- **Output format: 10-bit parallel RGB raw data**
- **On-chip 6-bit (1 sign bit+ 5 magnitude bit) background compensation DAC**
- **On-chip programmable gain amplifier**
  - **5-bit color gain amplifier(x4)**
  - **5-bit global gain amplifier (x5)**
- **Continuous variable frame time(1/2sec~1/30sec)**
- **Continuous variable exposure time**
- **I2C Interface**
- **Digitally programmable registers**
- **Single 3.3V supply voltage**
- **100 mW low power dissipation**

Key Specification

Supply Voltage	3.3V ± 5%
Array formate	356(H) x 292(V)
Optical format	~1/5 "
Pixel Size	7.25µm x 7.25µm
Frame rate	30 fps
System clock	Up to 48 MHz
Max. pixel rate	4 MHz
Sensitivity	1.0V/Lux-sec
PGA gain	31.6 dB max.
Color filter	RGB Bayer Pattern
Exposure Time	~ Frame time to 1/160000
Scan Mode	Progressive
S/N Ratio	>45dB
Package	32-pin LCC

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1. Pin Assignment

Pin No.	Name	Type	Definition
1	VSSA	GND	Analog ground
2	VRB	BYPASS	Analog voltage reference
3	VRT	BYPASS	Analog voltage reference
4	VCM	BYPASS	Analog voltage reference
5	VDDA	PWR	Analog VDD, 3.3V
6	VDDA	PWR	Analog VDD, 3.3V
7	VDDAY1	PWR	Analog VDD, 3.3V
8	VDDAY2	PWR	Analog VDD, 3.3V
9	VSSAY	GND	Analog ground
10	CSB	IN	Chip select (Low, active, chip disable if high)
11	PXD9	OUT	Digital data out
12	PXD8	OUT	Digital data out
13	PXD7	OUT	Digital data out
14	PXD6	OUT	Digital data out
15	PXD5	OUT	Digital data out
16	PXD4	OUT	Digital data out
17	VDDQ	PWR	Digital VDD, 3,3V
18	VSSQ	GND	Digital ground
19	PXD3	OUT	Digital data out
20	PXD2	OUT	Digital data out
21	PXD1	OUT	Digital data out
22	PXD0	OUT	Digital data out
23	PXCLK	OUT	Pixel clock output
24	HSYNC	OUT	Horizontal synchronization signal
25	VSYNC	OUT	Vertical synchronization signal
26	SYSCLK	IN	Master clock input
27	SCL	IN	I2C clock
28	SDA	I/O	I2C data
29	VDDD	PWR	Digital VDD, 3.3V
30	VSSD	GND	Digital ground
31	VSSA	GND	Analog ground
32	VLRST	BIAS	Fixed bias input voltage, 1.65V

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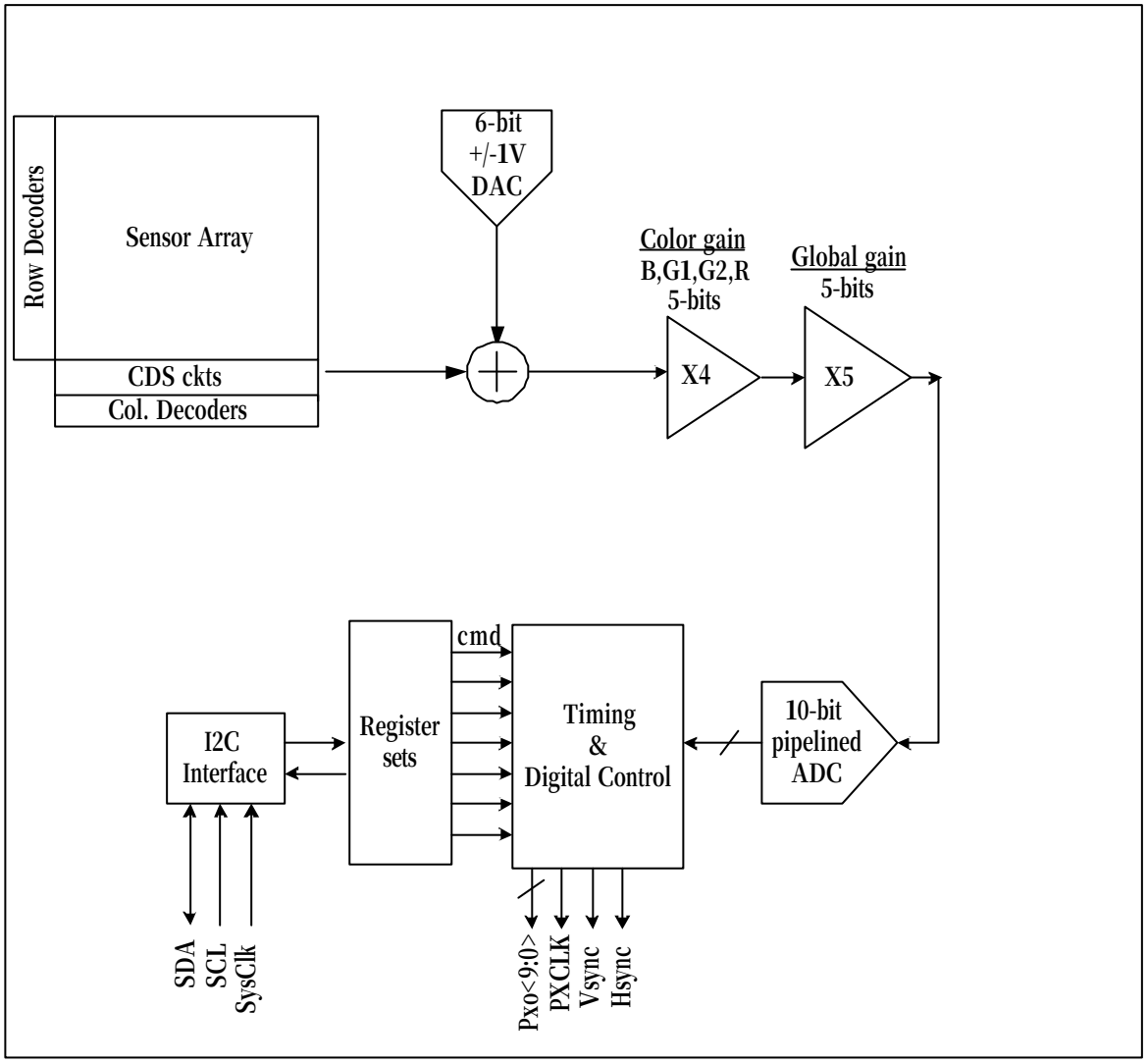
2. Block Diagram



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3. Pixel Array And Pixel Color Pattern

The output image format of PAS106BCA-323/PAS106BBA-323 is CIF (352x288 pixel array). To provide the co-processor with the extra information it needs for interpolation at the edges of the pixel array, an border of 2 pixels on all 4 sides of the array are available. Fig 3.1. illustrates the pixel array and pixel color pattern.

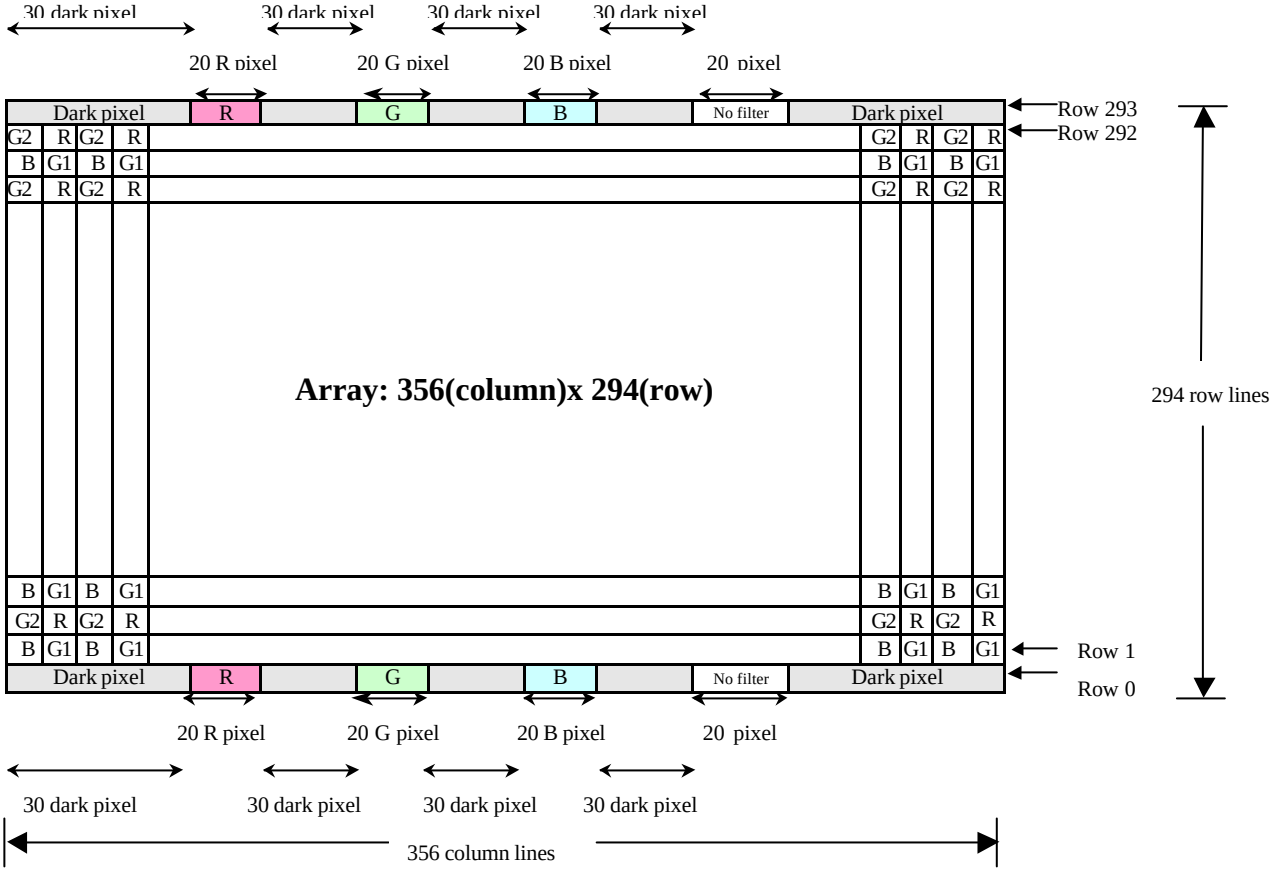

Fig 3.1. Pixel array and pixel color pattern

Note:

1. Pixel color pattern does not apply to monochrome sensor.
2. Pixel read-out proceeds from left to right, and from bottom row to top row.
3. Pixel array not drawn to scale.

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4. Output timing:

Fixed pixel clock for each line(row), 444pxclk.

4+4 blank pxclk for each line. (See Fig 4.1.)

1+1 Dark line for each frame.(See Fig 4.2.)

Dark line output format: Fig 4.3.

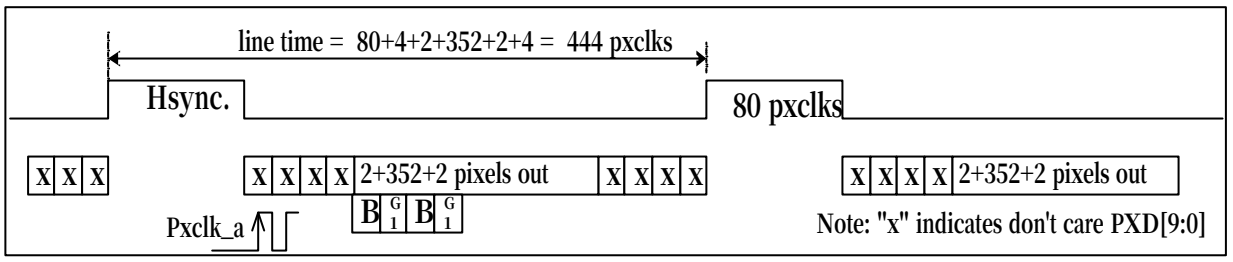

Fig 4.1. Inter-line timing

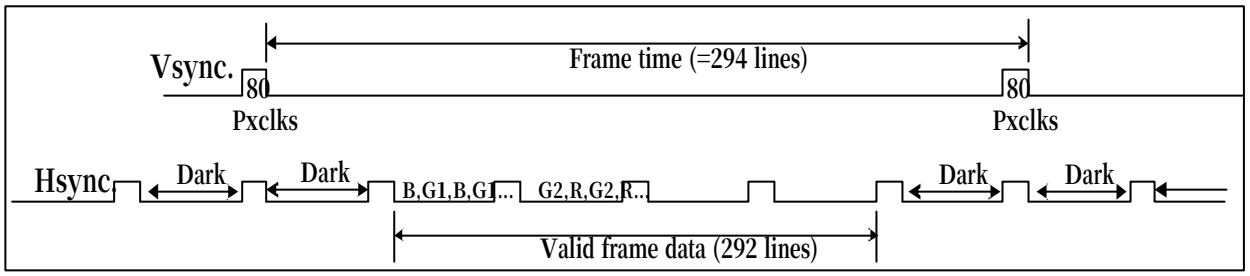

Fig 4.2. Inter-frame timing

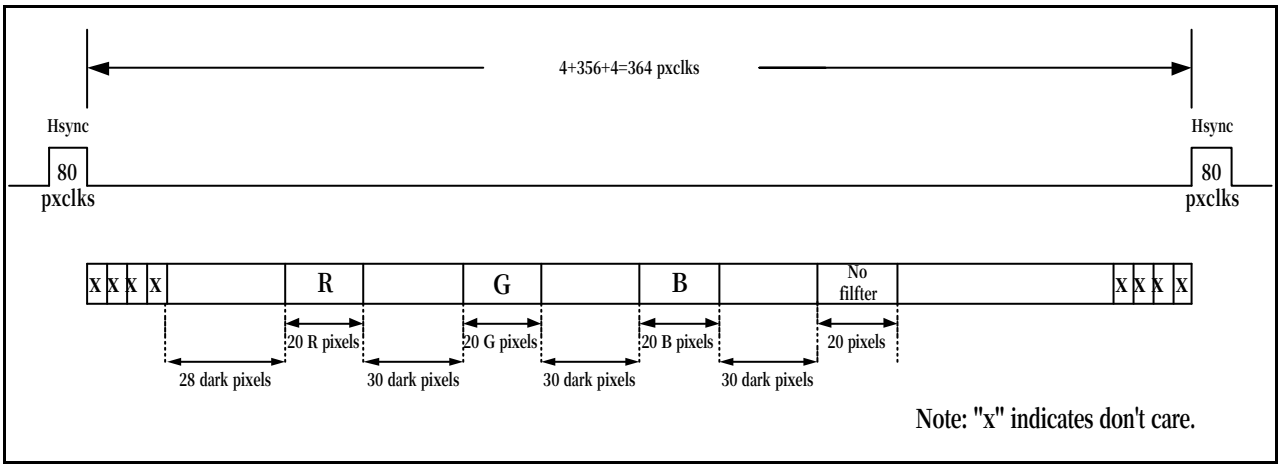

Fig 4.3. Dark line output format

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5. I2C Bus

PAS106BCA-323/PAS106BBA-323 supports I2C-bus transfer protocol and is acting as slave device. The 7 bits unique slave address is 1000000 and supports receiving / transmitting speed up to 400kHz.

5.1 I2C bus overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pull high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Fig 5.1.
- Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Please refer to Fig 5.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

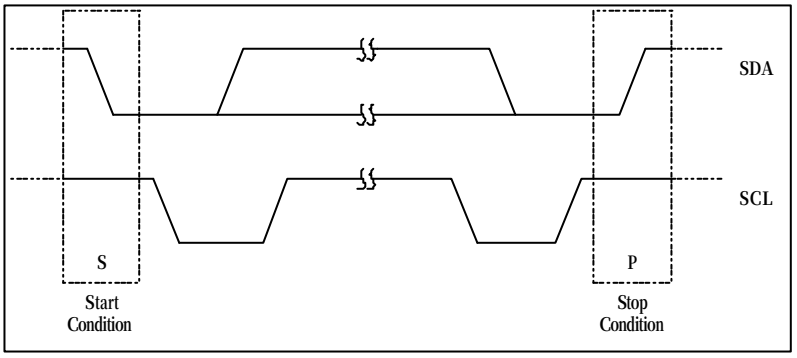

Fig 5.1 Start and Stop Conditions

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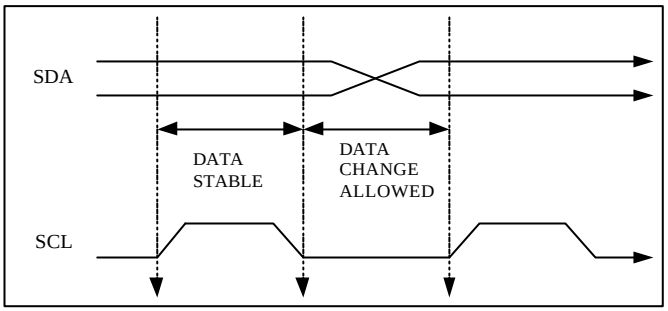
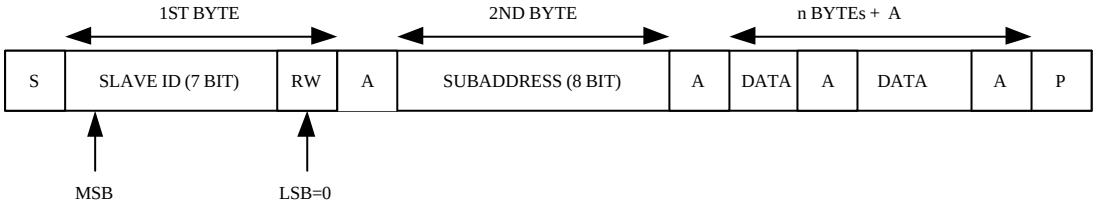


Fig 5.2 Valid Data

5.2 Data Transfer Format

5.2.1 Master transmits data to slave (write cycle)

- S : Start
- A : Acknowledge by slave
- P : Stop
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
  RW=1 read cycle, RW=0 write cycle.
- SUBADDRESS : The address values of PAS106BCA-323/PAS106BBA-323 internal control registers (Please refer to PAS106BCA-323/PAS106BBA-323 register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After slave(PAS106BCA-323/PAS106BBA-323) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. Again follow the PAS106BCA-323/PAS106BBA-323 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS106BCA-323/PAS106BBA-323 control register (address was assigned by 2nd byte). After PAS106BCA-323/PAS106BBA-323 issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS106BCA-323/PAS106BBA-323 sub-address is automatically increment after each DATA byte transferred.

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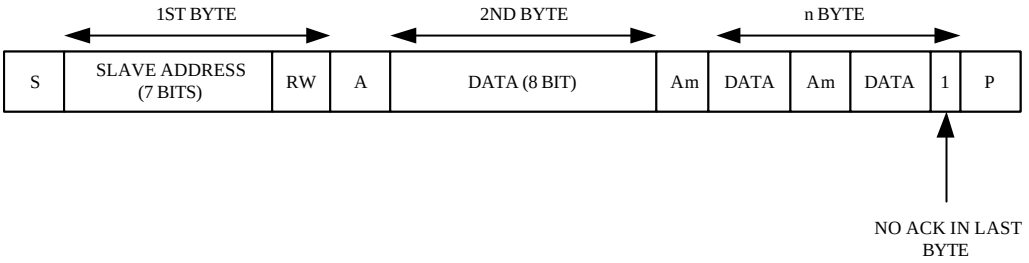
The data and A cycles is repeat until last byte write. Every control registers value inside PAS106BCA-323/PAS106BBA-323 can be programming via this way. (Please refer to Fig 5.3.)

5.2.2 Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle
- The sub-address is automatically increment after each byte read
- Am : Acknowledge by master
- Note there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS106BCA-323/PAS106BBA-323. The 8 bit data was read from PAS106BCA-323/PAS106BBA-323 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS106BCA-323/PAS106BBA-323 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS106BCA-323/PAS106BBA-323) must releases SDA line to master to generate STOP condition. (Please refer to Fig 5.3.)

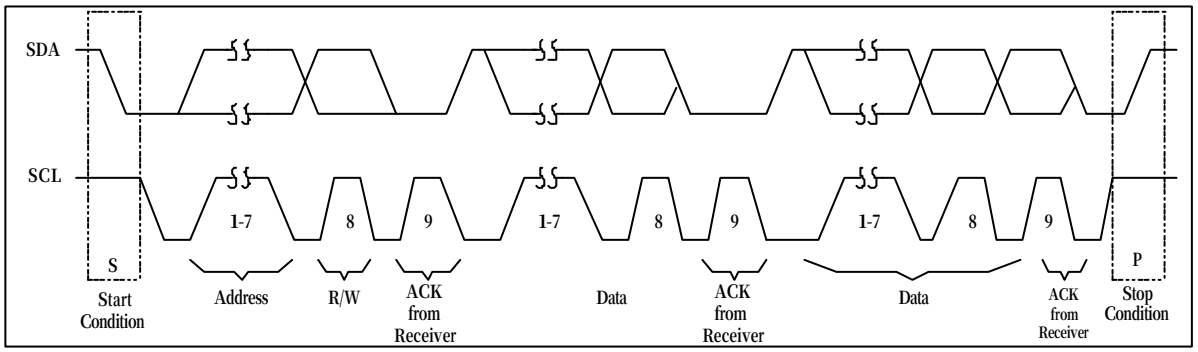


Fig 5.3 Data Transfer Format

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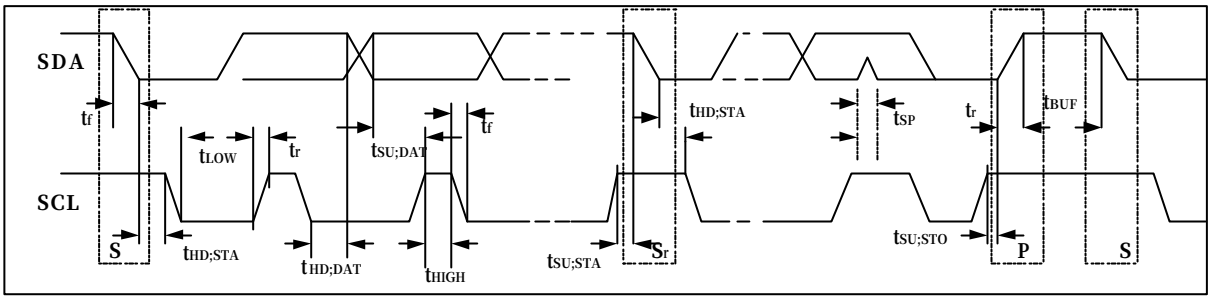
5.3 I2C Bus Timing



5.4 I2C Bus Timing Specification

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{scl}	10	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	us
HIGH period of the SCL clock	t_{HIGH}	0.75	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	us
Data hold time. For I2C-bus device	$t_{HD;DAT}$	0	3.45	us
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	30	N.D.	ns(note1)
Fall time of both SDA and SCL signals	t_f	30	N.D.	ns(note1)
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	us
Bus free time between a STOP and START	t_{BUF}	4.7	-	us
Capacitive load for each bus line	C_b	1	15	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	-	V

Note1: It depends on the "high" period time of SCL.

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6. Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vdd	DC supply voltage	-0.5	3.8	V
Vin	DC input voltage	0.5	Vdd+0.5	V
Vout	DC output voltage	-0.5	Vdd+0.5	V
Tstg	Storage temperature	0	70	℃

DC Electrical Characteristics (VDD=3.3V±5%, Ta=0°C~40°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
VDD	Analog and digital operating voltage	3.15	3.3	3.45	V
IDD	Operating Current		35		mA
Type :IN & I/O Reset and SYSCLK					
VIH	Input voltage HIGH	2.0		VDD	V
VIL	Input voltage LOW	0		0.8	V
Cin	Input capacitor			10	pF
Ilkg	Input leakage current			1.0	uA
Type : OUT & I/O for PXD0:9, PXCLK, H/VSYNC & SDA, load 10pf, 1.2kΩ, 3.3 volts					
VOH	Output voltage HIGH	Vdd-0.2			V
VOL	Output voltage LOW			0.2	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
fsysclk	Master clock frequency	8		48	MHz
fpxclk	Pixel clock output frequency			4	MHz

Sensor Characteristics (To be determined)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Photo response non-uniformity	PRNU		1.02		%	
Saturation output voltage	Vsat.		1.4		V	
Dark output voltage	Vdark		52		mV/sec	
Dark signal non-uniformity	DSNU		1.9		Lsb	
Sensitivity (Red channel)	R		1.2		V/Lux-sec	
Sensitivity (Green channel)	G		1.0		V/Lux-sec	
Sensitivity (Blue channel)	B		0.8		V/Lux-sec	

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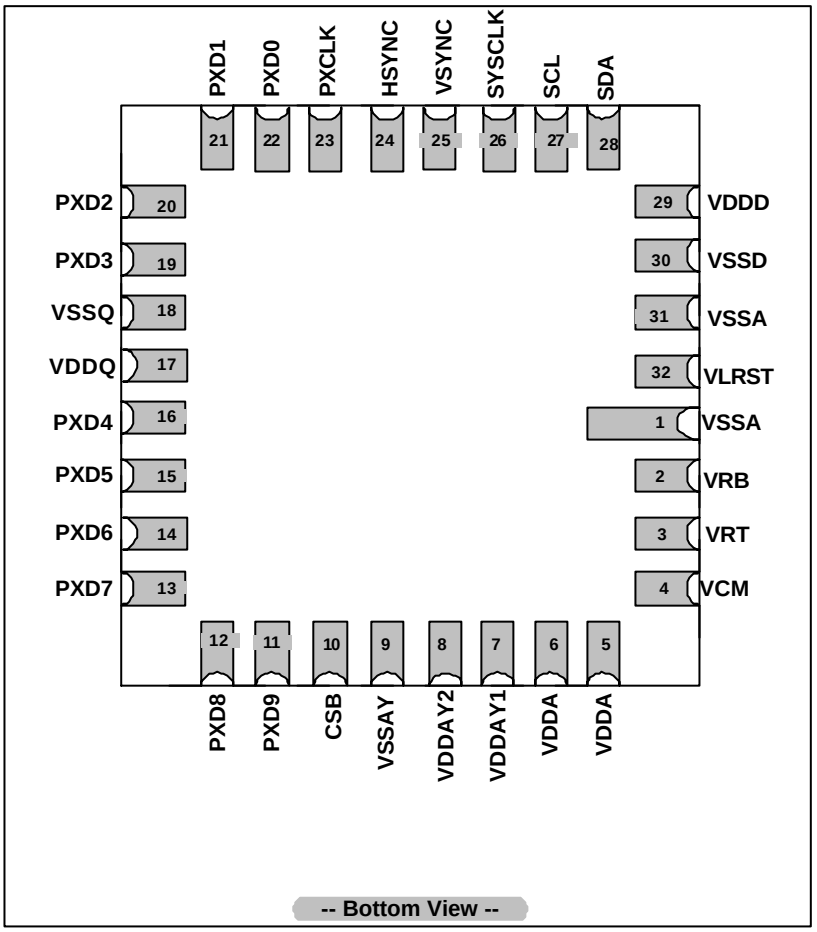
7. Package Information

7.1. Pin Connection Diagram



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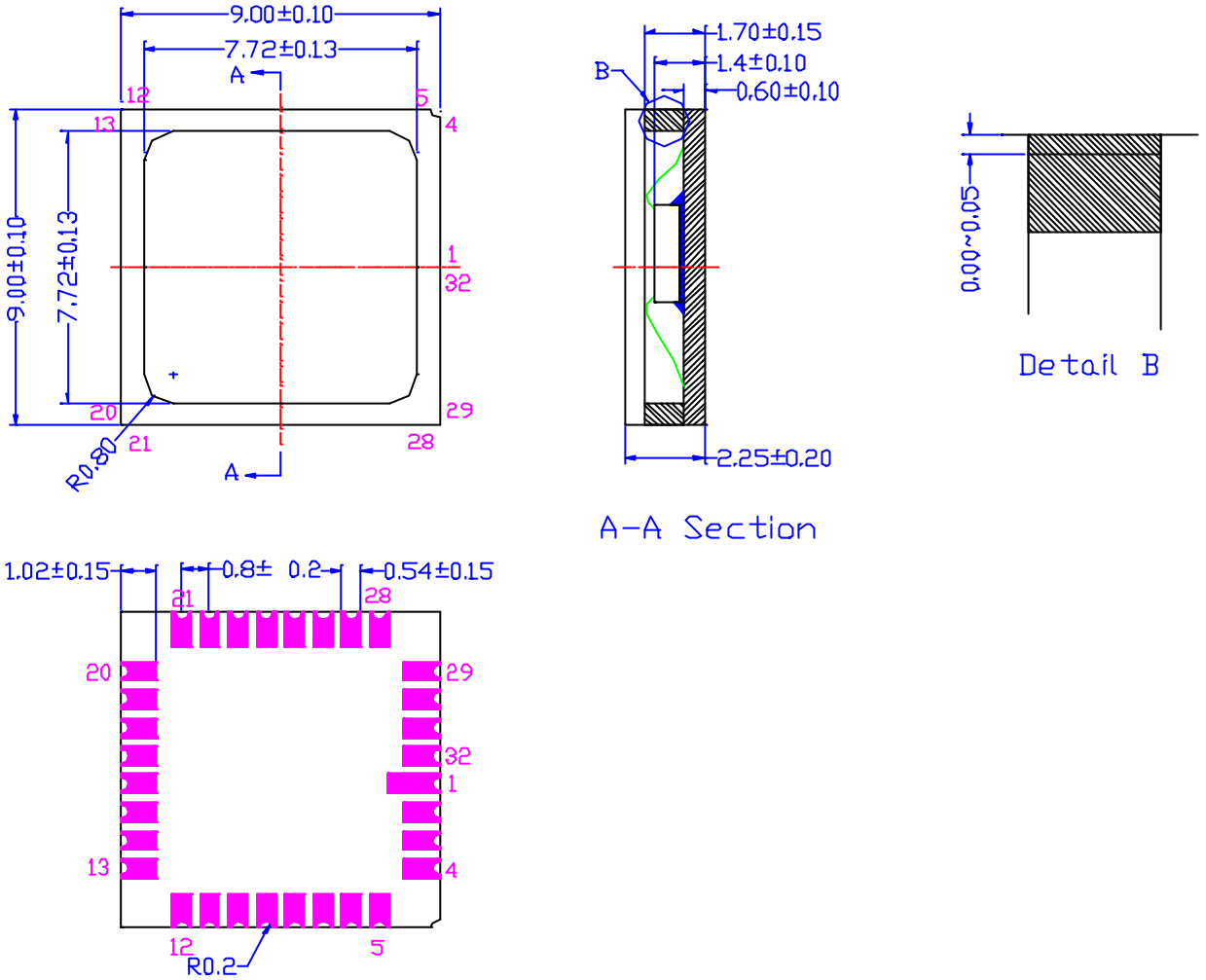
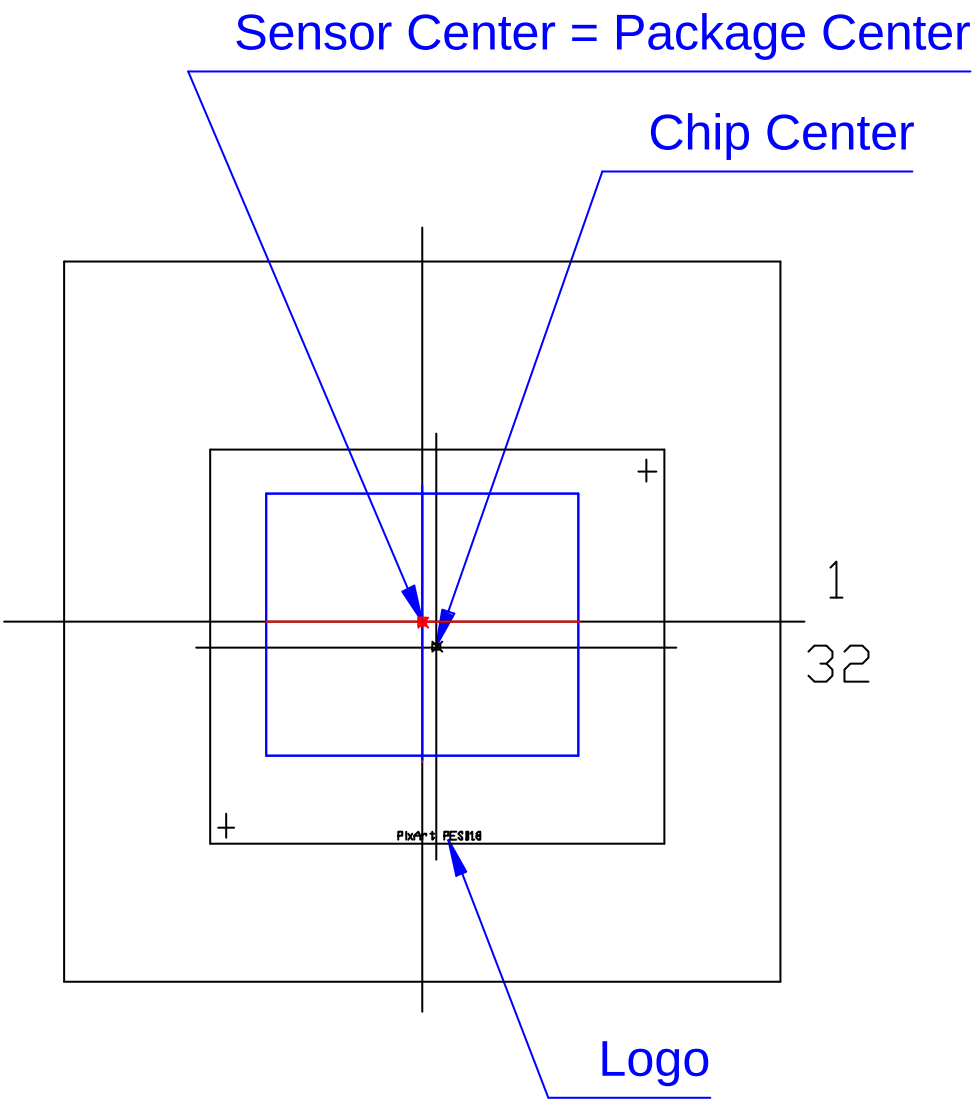
7.2. Package Outline



7.3. Sensor center and Die&Package center bias



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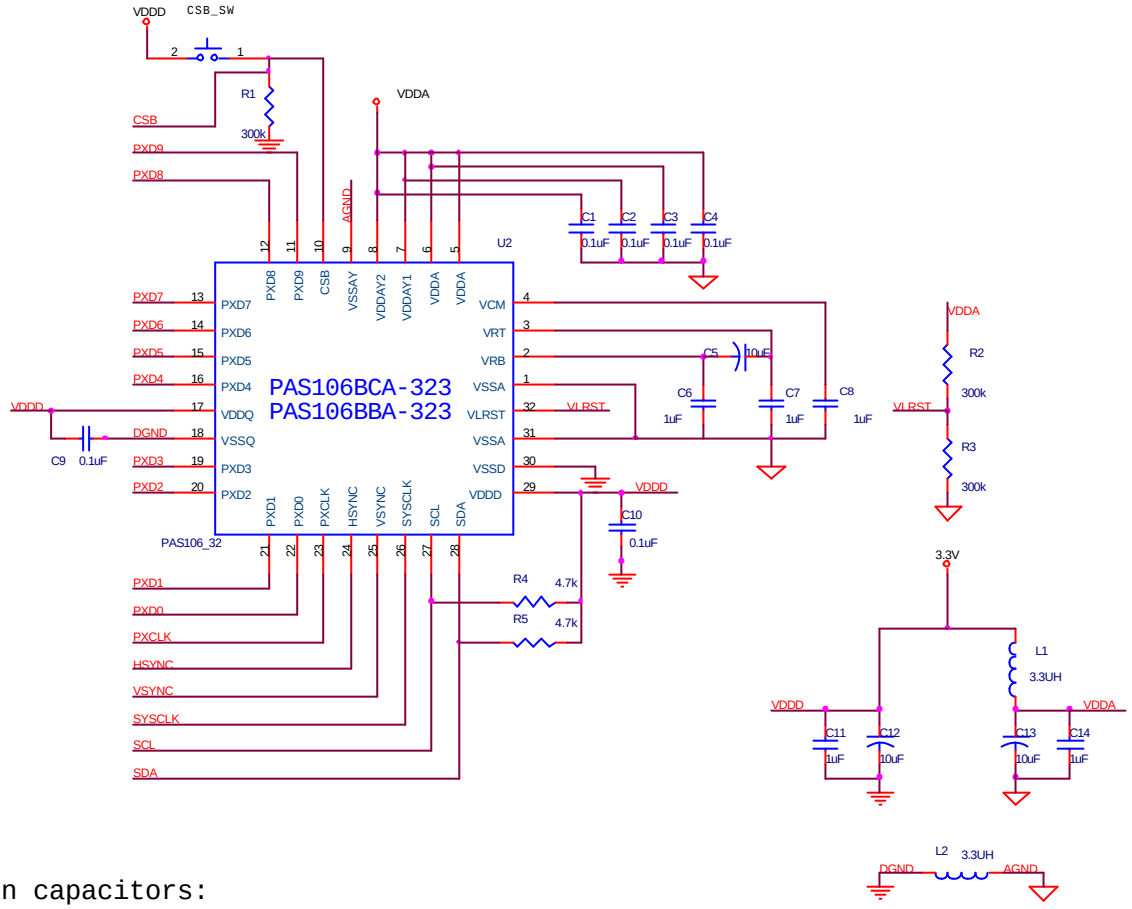
8. Referencing Circuit Schematic



NOTES on capacitors:

1.The 0.1uF caps for power pins MUST have trace lengths LESS than 5mm.

2.C5,C7 and C8 for pins 2,3 and 4 MUST have trace lengths LESS than 5mm.

Title	PAS106_SENSOR-32PINS.opj	
Size A4	Document Number	Rev V2.1
Date: Wednesday, May 22, 2002	Sheet 1 of 1	